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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,595	06/09/2005	Noriaki Chiba	HEIWA.026AUS	5434

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EXAMINER	
ISLA RODAS, RICHARD	
ART UNIT	PAPER NUMBER
2829	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,595	CHIBA, NORIAKI	
	Examiner	Art Unit	
	Richard Isla-Rodas	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent to Watanabe (6,226,230).

In terms of claim 1, Watanabe shows in Figure 14, a timing generation circuit comprising a timing memory (113C) containing predetermined timing data (each address location stores timing data) and a counter (14) for loading timing data output from the timing memory (bits of timing data stored in address locations of the timing memory) and outputting a pulse signal (P_{S1}, P_{S2}) at a timing indicated by the timing data (each bit of timing data DY_S and DY_R is used to determine rise timing and falling timing of the pulse TP as explained in lines 17-20, column 3), the timing generation circuit further comprising load data switching means (113D + 3D +11) for dividing a memory region (each bit in the plurality of bits stored in an address location is "divided" and sent separate bits to the counter 14 "one after the other") of the timing memory, selecting one timing data output (either MT) from the divided memory regions, and loading the selected one timing data in the counter (14) to thereby output the pulse signal (P_{S1}, P_{S2}) of one timing indicated by the one timing data.

As to claim 2, Watanabe also shows the timing generation circuit according to claim 1, wherein the load data switching means (113D + 3D +11) divides the memory region of the timing memory in an address direction by switching (the down counter outputs each bit in each address location in succession after each clock cycle REFCLK and thus outputs the bits by "switching" states), links a plurality of timing data output from the divided memory regions in a data bit width direction (the bits in the address location are output consecutively one after the next and thus in a row bit width direction), and loads these data as one timing data in the counter.

As to claim 3, Watanabe shows the timing generation circuit according to claim 1, wherein the load data switching means comprises an address selection circuit (113D) which designates one address of the timing memory (113C) and which outputs (through element 11) a plurality of timing data (a plurality of bits stored in each address location) stored in the corresponding one address and a load data switching circuit (11) which loads the one timing data (each separate bit) as such in one counter (14), when one timing data is output from the timing memory by switching (by switching states through each clock cycle), and which loads the plurality of timing data (a row of bits through a plurality of clock cycles) in a plurality of cascaded counters (14, 13 and 16), when a plurality of timing data are output from the timing memory by switching, to thereby output the pulse signal of one timing indicated by the one timing data (the timing data stored in the memory device 113C).

It must be noted that the recitation "by switching" is understood as the switch between states that is required for digital devices to output information. A clock signal (REFCLK) facilitates such switch between states.

As to claim 4 and 5, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ F.2d 1647 (1987).* Therefore, the recitation that the address selection circuitry "divides" and that the load switching circuit "loads" are recitation of the manner in which the structure is intended to be used. Since the claim does not recite structure new to independent claims 1 or 3, the recitation of intended use alone cannot be given patentable weight.

As to claim 6, Watanabe shows the load data switching means (113D + 3D +11) comprises a **data division circuit** (circuitry inside element 3D) which divides the timing data (all bits stored in one address location are output one at a time, thus dividing them) stored in one address of the designated timing memory (113C) into a plurality of timing data (a plurality of bits **see note below) and which outputs one timing data (one bit) among the plurality of divided timing data (divided bits), and a load data switching circuit (11) which loads the one timing data (each separate bit) as such in one counter (14), when one timing data is output from the timing memory by switching (by switching states through each clock cycle), and which loads the plurality of timing data (a row of bits after a plurality of clock cycles) in a plurality of cascaded counters (14, 13 and 16), when a plurality of timing data are output from the timing memory by switching, to

thereby output the pulse signal of one timing indicated by the one timing data (the timing data stored in the memory device 113C).

**It must be noted that each address location in 113C stores a plurality of bits (timing data) which are inputted to the summation processing device (3D) and then divided by a time duration (see lines 62-63 in column 3) the result of which (a plurality of bits) is outputted to the load data switching circuit (11).

As to claim 7, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ F.2d 1647 (1987).* Therefore, the recitation that the data division circuit "divides", "designates" and "outputs" and that the load switching circuit "loads" are recitation of the manner in which the structure is intended to be used. Since the claim does not recite structure new to independent claim 1 and 6, the recitation of intended use alone cannot be given patentable weight.

In terms of claim 8, it should be noted that a recitation with respect to the manner in which a claimed apparatus **(in this case the timing generating circuit disclosed by Watanabe)** is intended to be employed **(as part of a tester)** does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ F.2d 1647 (1987).* Also, a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations

are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Therefore, the preamble of claim 8 is not given patentable weight.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 8 is alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Watanabe (6,226,230) in view of the admitted prior art of Figure 10.

In terms of claim 8, Watanabe substantially shows all of the claimed elements of a timing signal generator, as recited in claim 1. Watanabe however, does not show a configuration of devices, including the timing generator which are used to test a device under test. However, the admitted prior art of Figure 10, shows a system for testing semiconductors, comprising a timing generation unit (1) connected to a pattern generator (2) which applies a signal to a device under test (M) and a comparator (4) that compared the signal generated with a the response signal of the device under test using. The admitted prior art teaches that it was well known in the art, at the time the application was filed, to arrange the aforementioned elements together with a timing generator, in order to test semiconductor devices. It would have been obvious to one of

the ordinary skill in the art, at the time of the invention, to use the timing generator disclosed by Watanabe as part of a test system as configured by the admitted prior art of Figure 10, in order to test Semiconductor Devices using delayed timing signals.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patents to Hiwada et al. (5,293,080), Uehara (5,854,798), Sudou et al. (6,903,566) and Watanabe (4,998,025).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Isla-Rodas whose telephone number is (571) 272-5056. The examiner can normally be reached on Monday through Friday 8 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Isla-Rodas
February 17, 2007

HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER